

A Surface Chemistry Approach to the Development of Gas Phase Wafer Cleaning Processes

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The International Technology Roadmap for Semiconductors (ITRS) identifies technical challenges for front-end of line (FEOL) surface cleaning in the areas of particle removal, hydrophobic and hydrophilic surface termination, and high κ compatible cleans. Options for both liquid and gas phase FEOL cleaning processes are shown in Table 1. Liquid phase cleaning is a mature and robust technology that offers the advantages of an aqueous solvent medium and high throughput, but is resource intensive. In addition to the liquid chemicals required, large amounts of water (60-80 million gallons per month for 20,000 wafer starts), cleanroom space for benches, and energy to run exhaust blowers are required. Moreover, wafer cleaning and CMP are the only semiconductor manufacturing processes that are carried out in a liquid phase, making them difficult to integrate with vacuum-based steps.

Table 1: FEOL Surface Cleaning Challenges and Processing Options (adapted from the 1999 ITRS).

Challenge	Processing Options	
	Liquid Phase	Gas Phase
Particle Removal	Dilute Chemistries Alternative Chemistries	Cryo Aerosol Laser
Hydrophobic Surface Termination	Integrated Final Rinse/Dry pH Adjusted Rinses Modified HF Chemistry	HF/vapor UV-Cl ₂
Hydrophilic Surface Termination	SC-1 + Chelating Agents Ozonated DIW Rinses	Ozone UV-Ozone
New High κ Dielectrics	<i>Under development</i>	<i>Under development</i>

Gas phase or dry cleaning processes offer the potential to reduce the environmental impact of wafer cleaning in the fab and provide technology options for the next generation of front-end processing. Dry cleans improve narrow geometry penetration, use much less chemistry, and, in principle, little or no water, and are vacuum compatible compared to aqueous based cleans. In spite of these obvious benefits, gas phase cleaning has not developed as initially envisioned due in large part to the continued improvement in liquid phase cleaning technology. A reduction in the feature size of devices, environmental regulations set by government and targets set by the ITRS Roadmap, as well as the adoption of a cluster tool concept and the introduction of new materials by the semiconductor industry are driving the development of new cleaning strategies. These new strategies often include dry cleans used in combination with aqueous based cleans for final surface conditioning before deposition. Whether dry cleaning is used to complement liquid phase cleaning or replace it, knowledge of the surface chemistry is key to process and reactor design as well as process control and optimization.

Both anhydrous HF alone and combined with vapor molecules and UV-initiated gas phase cleans are currently under study in our lab using a surface chemistry

approach. The reaction mechanisms for SiO₂ etching using HF/vapor mixtures and organic and metal atom removal using UV-Cl₂ are being investigated with *in situ* FTIR spectroscopy and ellipsometry in reactor modules as well as XPS and Auger in a surface analysis chamber connected by vacuum transfer. An integrated HF/vapor and UV-Cl₂ process is effective in removing organics and oxides after RIE and ashing, but submonolayer coverages of oxide and fluorine approaching one-half monolayer are typically left on the Si surface. UV-Cl₂ has also shown to be effective for removing some metals, such as Cu, Ni, and Fe. Etching and roughening can become significant at temperatures above 100°C, which is of concern because the volatility of metal chlorides is relatively low at lower temperatures. Etching does not appear to be a concern, however, with oxide surfaces. Metal atoms are typically easier to remove from silicon surfaces than from oxide surfaces due to the lower oxidation state of the metallic contamination. In addition to surface chemical mechanisms and reaction rates, the integration of these processes is under study as a pre-gate clean prior to the deposition of high κ materials proposed to replace SiO₂.

Another study involves etching of doped SiO₂ films used as insulating and sacrificial layers in the manufacture of microelectronic and MEMS devices. Gas phase HF etching of these films produces a residue with a low volatility. The residue layer is typically rinsed off with water before further processing. This water rinse, depending on the type of device structure produced, must be followed by an alcohol and/or supercritical CO₂ rinse and drying. The development of a completely gas phase etching process for doped oxides would eliminate these extra rinsing steps, thus decreasing the waste produced and potentially processing time. The chemical identity of the residue layers left on the surface after exposure to anhydrous HF is a function of the dopant atom in the oxide. The primary etching products in the condensed layer on PSG were found to be phosphoric acid, H₃PO₄, and water using FTIR spectroscopy. On BPSG a mixture of phosphoric and boric, B(OH)₃, acids and water was produced. The reaction of boric oxide, B₂O₃, crystallites with water to produce B(OH)₃ is thermodynamically favorable and should react further to boron trifluoride, BF₃, in the presence of HF. The formation of B(OH)₃ rather than BF₃ in the etching residue on BPSG indicates that a kinetic limitation exists due to either the relatively low HF exposure used or the chemistry within the mixed acid film. The etching product in the residue on BSG, which was exposed to a higher HF flux, was primarily boron trifluoride dihydrate, BF₃•2H₂O. The condensed layer supports the etching of the Si-O matrix by concentrating the HF and water reactants close to the surface, which explains the enhancement in the etching rate when a condensed layer is formed. The etching products identified by FTIR could also play a direct role in the etching reaction since hydroxyl groups on the acids can activate Si-O bonds similar to water and the Lewis acid BF₃ can attach to Si-O via the pair of electrons on the O atom (Figure 1).

Figure 1: Proposed activation of SiO₂ matrix by BF₃ during HF etching.

